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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/813,433	KNOWLES, SIMON	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-29 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: RCE, Extension of Time, and Amendment as received on 6/11/2007.

Claim Objections

3. Claim 12 is objected to because of the following informalities: The dependency of claim 12 is unclear as applicant claims that claim 12 is dependent on "any of claim 9". It is not clear if applicant desires claim 12 to be dependent on claim 9 or on more than just claim 9. For purposes of examination, the examiner will assume applicant meant the former. Appropriate correction is required.

4. Claim 22 recites the limitation "the results" in the last line of the claim. There is a lack of antecedent basis for this limitation in the claim as it is not clear what the results are. It is asked that applicant clarify, but the examiner will assume that the results are meant to be those produced by the execution paths. Appropriate correction is required.

5. Claim 23 recites the limitation "the results" in the last line of the claim. There is a lack of antecedent basis for this limitation in the claim as it is not clear what the results are. It is asked that applicant clarify, but the examiner will assume that the results are meant to be those produced by the execution paths. Appropriate correction is required.

6. Claim 24 is objected to because of the following informalities: In lines 2 and 3, insert --of-- after "first plurality" and "second plurality", respectively. Appropriate correction is required.

7. Claim 25 is objected to because of the following informalities: In line 4, applicant refers to converting "relatively bits". This is grammatically incorrect and must be reworded. For purposes of examination, the examiner will read "relatively bits" as --bits--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 11 and 25-28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. The term "relative interconnectivity" in claim 11 is a relative term which renders the claim indefinite. The term "relative" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

11. The terms "relatively bits" and "relatively complex configuration settings" in claim 25 are relative terms which render the claim indefinite. The term "relatively" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

12. Claims 26-28 are rejected under 35 U.S.C 112, 2nd paragraph, for being indefinite, because they are dependent, either directly or indirectly, on an indefinite claim.

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

14. Claims 22-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Trimberger, U.S. Patent No. 5,737,631.

15. Referring to claim 22, Trimberger has taught a method of operating a computer processor having control and data processing capabilities, said computer processor comprising a control execution path (for instance the path from instruction register 111 to decoder 112 is a control execution path because the instruction passed to the decoder along this path controls execution), a first data execution path including fixed operators and a second data execution path including configurable operators (Fig.2, item 100), said configurable operators having a plurality of predefined configurations (Fig.2, item 120), at least some of which are selectable by means of an opcode portion of a data processing instruction (Trimberger: column 2, lines 62-67; column 3, lines 1-9), the method comprising:

a) decoding a plurality of instructions to detect whether at least one data processing instruction, of said plurality of instructions, defines a fixed data processing operation or a configurable data processing operation (Trimberger: column 7, lines 45-50);

b) causing the computer processor to supply data for processing to said first data execution path when a fixed data processing instruction is detected and to said configurable data execution path when a configurable data processing instruction is detected; and outputting the results (Trimberger: column 7, lines 45-50).

16. Referring to claim 23, Trimberger has taught a computer program product comprising program code means for causing a computer processor, said computer processor comprising a control execution path having its own control register (see Fiug.2 and note that components 111, 112, 105, 106, 115, may be considered part of the control execution path as these components control which instruction is fetched, decoded, and ultimately executed. The path includes at least control register 111 which holds the instruction to be decoded.), a first data execution path (Fig.2, component 100) including fixed operators and a second data execution path (Fig.2, component 120) including configurable operators, said configurable operators having a plurality of predefined configurations, at least some of which are selectable by means of an opcode portion of a data processing instruction (Trimberger: column 2, lines 62-67; column 3, lines 1-9), to:

a) decode a plurality of instructions to detect whether at least one data processing instruction, of said plurality of instructions, defines a fixed data processing operation or a configurable data processing operation (Trimberger: column 7, lines 45-50);

b) cause the computer processor to supply data for processing to said first data execution path when a fixed data processing instruction is detected and to said configurable data execution path when a configurable data processing instruction is detected; and output the results (Trimberger: column 7, lines 45-50).

17. Claim 29 is rejected under 35 U.S.C. 102(b) as being anticipated by Hull et al., U.S. Patent No. 5,922,065 (herein referred to as Hull).

18. Referring to claim 29, Hull has taught a computer processor having control and data processing capabilities comprising:

a) a decode unit configured to identify instruction packets as a first type of instruction packet containing only control instructions, or as a second type of instruction packet containing at least one data instruction and at least one memory instruction, or as a third type of instruction packet containing at least one data instruction and at least one control instruction. See Fig.4 and note the templates. Also note that a decoder is inherent in any computing system to determine the operation types. Finally, it should be noted that applicant's claim is written in alternative form and therefore, even if only one of the alternatives is taught by the prior art the claim is anticipated. In Hull, data instructions would be at least I and F instructions, a control instruction would be at least a B instruction, and a memory instruction would be at least an M instruction.

b) a control execution unit for executing control instructions and a data executing unit for executing data instructions and memory instructions. Clearly, if the instructions exist, then an appropriate execution unit must exist to perform the execution.

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claims 1-21 and 24-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Trimberger.

21. Referring to claim 1, Trimberger has taught a computer processor having control and data processing capabilities comprising:

a) a decode unit for decoding instructions (Trimberger: Figure 2, item 112);

b) a dedicated data processing facility having its own data register file (Fig.2, component 103 or 130), the data processing facility comprising a first data execution path including fixed operators (Trimberger: Figure 2, item 100) and a second data execution path including at least configurable operators (Trimberger: Figure 2, item 120), said configurable operators having a plurality of predefined configurations, at least some of which are selectable by means of an opcode portion of a data processing instruction (Trimberger: column 2, lines 62-67; column 3, lines 1-9; Figure 3, item 201);

c) wherein said decode unit is operable to detect whether a data processing instruction defines a fixed data processing operation or a configurable data processing operation, said decode unit causing the computer system to supply data for processing to said first data execution path when a fixed data processing instruction is detected and to said configurable data execution path when a configurable data processing instruction is detected (Trimberger: column 7, lines 45-50).

d) Trimberger has not taught a dedicated control processing facility comprising a control execution path having its own control register file. However, Official Notice is taken that branch units pushing return addresses on a stack-based register file is a well known and advantageous concept in the art. Specifically, a branch unit is a unit which controls program flow in response to a branch, such as a subroutine call or return instruction.

Having these instructions is useful because it allows the programmer to repeat a code routine by simply calling the routine. Without a call/return, each time the routine is to be repeated, the actual routine would have to be duplicated. Consequently, by having call/return instructions, code density is increased by only having to write the routine once. Furthermore, in response to such a call, the branch unit will push a return address into its register file stack, which is also a well known component. In response to a return from subroutine instruction, an address would be retrieved from the top of the register file stack. Note that such a register file stack is known to be used in return address prediction which is clearly useful because a return address may be predicted by the register file stack before the true address is fetched from main memory, thereby allowing the processor to continue execution without stalling (which in turn increase throughput). As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Trimberger to include a branch unit having its own register file for executing call and return-type instructions, and predicting return addresses to increase throughput. It should further be noted that such a register file is only written to and read from when a branch of some sort occurs, and consequently, it can be said that the branch unit has its own register file.

22. Referring to claim 2, Trimberger has taught a computer processor according to claim 1, wherein the decode unit is capable of decoding a stream of instruction packets from memory, each packet comprising a plurality of instructions (Trimberger: column 7, lines 51-56).

23. Referring to claim 3, Trimberger has taught a computer processor according to claim 1, wherein the decode unit is operable to detect if an instruction packet contains a data processing instruction (Trimberger: column 7, lines 45-50).

24. Referring to claim 4, Trimberger has taught a computer processor according to claim 1, wherein the configurable operators are configurable at the level of multibit values (Trimberger: column 9, lines 18-19) (The opcode is a multibit value).

25. Referring to claim 5, Trimberger has taught a computer processor according to claim 4, wherein the configurable operators are configurable at the level of multibit values comprising four or more bits (Trimberger: column 9, lines 18-19) (The opcode is at least 4 bits).

26. Referring to claim 6, Trimberger has taught a computer processor according to claim 4, wherein the configurable operators are configurable at the level of words (Trimberger: column 9, lines 24-25) (Immediate values are optional; therefore, the whole word is configurable).

27. Referring to claim 7, Trimberger has taught a computer processor according to claim 1. Trimberger has not taught that a plurality of the fixed operators of the first data execution path is arranged to perform a plurality of fixed operations in independent lanes according to single instruction multiple data principles. However, Official Notice is taken that SIMD and the related advantages are well known and accepted in the art. Specifically, SIMD allows each execution unit to perform the same instruction on different data in the same cycle, thereby increasing data level parallelism. Higher parallelism will potentially result in higher throughput as more operations can occur at once. Consequently, it would have been obvious to one of ordinary skill in the art at the

time of the invention to modify Trimberger such that a plurality of the fixed operators of the first data execution path is arranged to perform a plurality of fixed operations in independent lanes according to single instruction multiple data principles.

28. Referring to claim 8, Trimberger has taught a computer processor according to claim 1. Trimberger has not taught that a plurality of the configurable operators of the second data execution path is arranged to perform multiple operations in different lanes according to single instruction multiple data principles. However, Official Notice is taken that SIMD and the related advantages are well known and accepted in the art. Specifically, SIMD allows each execution unit to perform the same instruction on different data in the same cycle, thereby increasing data level parallelism. Higher parallelism will potentially result in higher throughput as more operations can occur at once. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Trimberger such that a plurality of the configurable operators of the second data execution path is arranged to perform multiple operations in different lanes according to single instruction multiple data principles.

29. Referring to claim 9, Trimberger has taught a computer processor according to claim 1, wherein configurable operators of the second execution path are arranged to receive configuration information which determines the nature of the operations performed (Trimberger: column 8, lines 5-17).

30. Referring to claim 10, Trimberger has taught a computer processor according to claim 9, wherein configurable operators of the second execution path are arranged to receive configuration information which determines the nature of the operations

performed from a field of an instruction defining a configurable data processing operation (Trimberger: column 7, lines 62-67; column 8, lines 1-17).

31. Referring to claim 11, Trimberger has taught a computer processor according to claim 1, wherein configurable operators of the second execution path are arranged to receive configuration information comprising information controlling relative interconnectivity (Trimberger: column 8, lines 35-37).

32. Referring to claim 12, Trimberger has taught a computer processor according to claim 9, comprising a control map associated with configurable operators of the second data execution path, said control map being operable to receive at least one configuration bit from a configurable data processing instruction and to provide configuration information to the configurable operators responsive thereto (Trimberger: column 7, lines 62-67; column 8, lines 1-17).

33. Referring to claim 13, Trimberger has taught a computer processor according to claim 12, wherein said configuration information controls interconnectivity between two or more of said configurable operators (Trimberger: column 8, lines 35-37).

34. Referring to claim 14, Trimberger has taught a computer processor according to claim 1, wherein configurable operators of the second execution path are arranged to receive either configuration information determining the nature of an operation to be performed or configuration information controlling interconnectivity from a source other than a configurable data processing instruction (Trimberger: column 8, lines 5-17; Figure 2; items 101, 102 and 123).

35. Referring to claim 15, Trimberger has taught a computer processor according to claim 1, wherein at least one configurable operator of the second data execution path is

capable of executing data processing instructions with an execution depth greater than two computations before returning results to a results store (Trimberger: column 3, lines 10-27) (It is inherent that these complex functions will take at least two cycles).

36. Referring to claim 16, Trimberger has taught a computer processor according to claim 1, comprising a switch mechanism for receiving data processing operands from a configurable data processing instruction and switching them as appropriate for supply to one or more of said configurable operators (Trimberger: column 7, lines 45-50).

37. Referring to claim 17, Trimberger has taught a computer processor according to claim 1, comprising a switch mechanism for receiving results from one or more of said configurable operators and switching the results as appropriate for supply to one or more of a result store and feed back loop (Trimberger: column 8, lines 51-59).

38. Referring to claim 18, Trimberger has taught a computer processor according to claim 1, comprising a plurality of control maps for mapping configuration bits received from configurable data processing instructions to configuration information for supply to configurable operators of the second data execution path (Trimberger: column 3, lines 66-67; column 4, lines 1-10).

39. Referring to claim 19, Trimberger has taught a computer processor according to claim 1, comprising a switch mechanism for receiving configuration information from a control map and switching it as appropriate for supply to configurable operators of the second data execution path (Trimberger: column 8, lines 5-17).

40. Referring to claim 20, Trimberger has taught a computer processor according to claim 1, comprising configurable operators selected from one or more of: multiply

accumulate operators; arithmetic operators; state operators; and cross-lane permuters (Trimberger: column 3, lines 10-27).

41. Referring to claim 21, Trimberger has taught a computer processor according to claim 1, comprising operators and an instruction set capable of performing one or more operations selected from: Fast Fourier Transforms; Inverse Fast Fourier Transforms; Viterbi encoding/decoding; Turbo encoding/decoding; and Finite Impulse Response calculations; and any other Correlations or Convolutions (Trimberger: column 3, lines 10-27) (polynomial evaluation is used in FFT and IFFT).

42. Referring to claim 24, Trimberger has taught a computer readable medium comprising an instruction set, said instruction set comprising a second plurality of instructions having a field indicating a fixed type of data processing operation and a third plurality of instructions having a field indicating a configurable type of data processing operations (Trimberger: column 9, lines 4-18).

a) Trimberger has not taught a first plurality of instructions having a field indicating a control processing operation. However, Official Notice is taken that program control flow execution units, i.e. branching execution units, and their benefits are well documented in the art. Branch units, in response to branch instructions, allow a processor to conditionally or unconditionally jump from one section of code to another, thereby allowing different code to be executed depending on the state of the program. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Trimberger to include a branch unit and multiple branch control instructions (unconditional, conditional, call, return, all of which are known) for

performing branching. It follows that a control instruction will inherently include a unique opcode field which specifies that it is a branch.

43. Referring to claim 25, Trimberger has taught a computer processor having a data execution path comprising configurable operators, wherein the configurable operators comprise a plurality of pre-defined groups of operator configurations, each group comprising operators from a separate operator class (Trimberger: column 2, lines 62-67; column 3, lines 1-27).

a) Trimberger has not explicitly taught a look-up table to convert relatively bits in an instruction into a set of relatively complex configuration settings for said configurable operators. However, Trimberger has taught that the function specified by the configurable operator is kept in the "immediate" field 261 (Trimberger: column 9, lines 38-39). Based on the contents of this field, the operands are routed to the reconfigurable logic to complete the function. With regular, fixed functions, the decoding and routing for an operator is done in one of two ways - 1. hardwiring, or 2. a lookup table. Based on the contents of the lookup table, the decoder knows where to route operands. With configurable operators, it is impossible to have the routing hardwired since the routing is not known at the time of design. Therefore, a lookup table is necessary. Consequently, although Trimberger does not explicitly teach a look-up table to convert relatively bits in an instruction into a set of relatively complex configuration settings for said configurable operators, the examiner takes official notice that such would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention since it is a viable solution to route configurable operators in a processor.

44. Referring to claim 26, Trimberger has taught a computer processor according to claim 25, wherein the operator classes comprise classes selected from one or more of: multiply accumulate operators; arithmetic operators; state operators; and permuters (Trimberger: column 3, lines 10-27).

45. Referring to claim 27, Trimberger has taught a computer processor according to claim 25, wherein connections between operators selected from within each of the pre-defined groups of operator configurations are capable of being configured by an opcode portion within an instruction executed by the computer processor (Trimberger: column 2, lines 62-67; column 3, lines 1-9; Figure 3, item 201).

46. Referring to claim 28, Trimberger has taught a computer processor according to claim 25, wherein connections between operators selected from more than one of the pre-defined groups of operator configurations are capable of being configured by an opcode portion within an instruction executed by the computer processor.

While not explicitly stated, such is inherent since the functions defined by Trimberger have overlapping logic (e.g. searching in a document and spell checking will have much of the same logic). Redundant logic on a large function is wasteful. Therefore, the bitmaps are broken up into smaller functions which can be shared by larger functions.

Response to Arguments

47. Applicant's arguments with respect to claims 1-28 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DJH
David J. Huisman
July 19, 2007